RCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/575,456	05/22/2000	James S. Cullum	M4065.0244/P244	2124

24998 7590 11/04/2004

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
1177AVENUE OF THE AMERICAS (6TH AVE)
NEW YORK, NY 10036-2417

EXAMINER	
TRUJILLO, JAMES K	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 11/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/575,456	CULLUM ET AL.	
	Examiner	Art Unit	
	James K. Trujillo	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,10-13,15,16,19,20,24-27,29,30,33,34,38-43,45-47 and 49-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 1,2,5,6,10-13,15,16,19,20,24-27,29,30,33,34,38 43,45-47 and 49-52.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Request for reconsideration dated 9/9/09.

2. Claims 1-2, 5-6, 10-13, 15-16, 19-20, 24-27, 29-30, 33-34, 38-43, 45-47 and 49-52 are presented for examination.

Claim Rejections

3. The rejections are respectfully maintained and reproduced infra for applicant's convenience.

4. Claims 1-2, 5-6, 10-13, 15-16, 19-20, 24-27, 29-30, 33-34, 38-43, 45-47 and 49-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (hereinafter AAPA) in view of Ashuri U.S. Patent 5,652,530 (hereinafter Ashuri).

5. As to claim 1, AAPA substantially taught the invention as per claim 1 including:

a. a clock source for supplying a first clock signal [17 figure 1];

b. a plurality of output circuits each of which receives and outputs a respective data signal, each said output circuit operating in response to a respective applied clock signal [13a-13n figure 1];

AAPA does not expressly teach a plurality of adjustable delay circuits for receiving said first clock signal, each said of adjustable delay circuit providing a respective delay first clock signal to a respective one of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the

respective clock signal, and wherein each programming circuit contains at least one fuse element for programming.

In summary, AAPA taught using a single delay for a clock for a plurality of output circuits wherein each output circuit has different data signal coupled to it input. The single delay of AAPA is not explicitly described in detail.

Ashuri, teaches a single output circuit having its own adjustable delay (delay shifter 310) providing a respective delayed first clock signal (from external clock 321) to an output circuit (flip-flop 350), wherein each adjustable delay circuit contains a programming circuit (fuses 520 and capacitors 530) for programming a respective delay to be applied to the respective clock signal, and wherein each programming circuit contains at least one fuse element (fuse elements 520) for programming [figures 3 and 5 and corresponding text]. In summary, Ashuri teaches an apparatus having a particular data signal for an output circuit that also has an associated adjustable delay [col. 1 lines 47-52]. The invention of Ashuri ensures that a clock signal is delayed by an appropriate amount relative to a delay with associated data signal.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify AAPA by removing the single delay of AAPA and placing a delay as taught by Ashuri for each output circuit into the respective clock line because both AAPA and Ashuri are directed toward placing delay into a clock signal. In making the modification the delay for each clock would be equal to a corresponding delay of the data signal. Therefore, in making the modification using the teachings of Ashuri into AAPA would suggest to one of ordinary skill that the each of said respective data signals would be output by said plurality of output circuits at substantially the same time. This modification results in the applicants claimed invention. That

is, each output circuit has it own associated adjustable delay circuit that is equal to the total delay for each data signal line. An artisan would have made the modification because Ashuri teaches that in his invention that a clock signal will (and should) be delayed by an appropriate amount for each data signal. Ashuri further teaches that the adjustable delay for the clock is desirable because it allows the data signal to be sampled at an appropriate time and that the delay is adjustable to accommodate different amounts of propagation delay for a particular data signal [col. 1 lines 21-60].

6. As to claim 2, AAPA combined with Ashuri taught the data output apparatus according to claim 1, described above. Ashuri further taught wherein each of the output circuits has an associated output data hold time, the timing of which is adjusted by the delay of a respective delay circuit [figure 3 col. 3 lines 13-23]. Ashuri teaches that the delay added should correspond to the delay in the particular data line.

7. As to claim 5, AAPA combined with Ashuri taught the data output apparatus according to claim 2, described above. As to claim 5, AAPA teaches that the output circuits would be connected to data output terminals because the output circuit are used to place output to a memory device thus requiring output terminals [page 2 lines 1-2]. AAPA together with Ashuri do not expressly disclose wherein the delay of each of said adjustable delay circuits is adjusted such that time of said data hold time of each of said output circuits is substantially coincident. However, because the delay as taught by Ashuri is now implemented in each clock path wherein each of the adjustable delay circuits is adjusted accordingly. Each output circuit signal path length differences and other timing aberrations caused by the circuit topology within the chip, as described by AAPA, are now compensated by the modification with Ashuri. Therefore, it would

have been obvious to one of ordinary skill in the art at the time of the invention to make the data hold time of each output circuit is now substantially coincident because doing so would allow the plurality of data signal to be aligned, which is desirable in AAPA to reduce the time to output the data to a device.

8. As to claim 6, AAPA together with Ashuri taught the data output apparatus according to claim 1, described above. AAPA combined with Ashuri further wherein each of said delay element comprises:

a. an input (input to delay shifter 510) for receiving said first clock signal [Ashuri – figure 5];

b. a plurality of delay elements (capacitors 530), each of said delay elements providing different respective delay to a signal applied thereto [Ashuri - figure 5 and corresponding text]; and

c. a switch circuit (control lines for selecting fuses 520) for selectively causing a selected one of said delay elements to delay said first clock signal and apply a delayed first clock signal to respective output circuit [Ashuri - figure 5 and corresponding text].

9. As to claim 10, AAPA together with Ashuri taught the data output apparatus according to claim 6, described above. Ashuri further taught wherein said switch circuit comprises a plurality of switch elements (selecting control lines to select fuses 520) respectively coupled to said plurality of delay elements (capacitors 530), one of said switch elements being selectively enabled to apply said first clock signal to its respectively coupled delay element [figure 5 and related text].

10. As to claim 11, AAPA together with Ashuri taught the data output apparatus according to claim 10, described above. Ashuri further taught comprising a programmable circuit for programming which of said switch elements (control lines are selected to enable/disable the fuses) is selectively enabled [col. 3 lines 47-53]. Ashuri suggests that a programmable circuit is user to selective enable switch elements by disclosing that that control lines may be used to allow a user to select fuses.

11. As to claim 12, AAPA together with Ashuri taught the data output apparatus according to claim 1, described above. AAPA further taught wherein the output circuits are output buffer circuits [AAPA - figure 1].

12. As to claim 13, AAPA together with Ashuri taught the data output apparatus according to claim 1, described above. AAPA further taught wherein each of said output circuits receives and outputs a respective data signal from a memory array [figure 1 and pages 1 line 11 through page 3 line 2].

13. As to claims 15-16, 18-20, 24-27, 29-30, 32-34 and 38-40, AAPA together with Ashuri taught the claimed data output apparatus therefore they also teach the claimed processor based system and the claimed memory device.

14. As to claim 41, AAPA taught a method of providing data output signal comprising:

a. receiving a plurality of data output signals at respective output circuits [figure 1];

b. operating said output circuits in response to respective applied clock signals to make data output signals available at the output of said output circuits [pages 1 line 11 through page 3 line 2].

c. providing a first clock signal [clock 17, figure 1];

AAPA does not expressly teach generating each said respective applied clock signal from said first clock signal, each respective applied clock signal having a respective adjustable delay relative to said first clock signal.

In summary, AAPA taught using a single delay for a clock for a plurality of output circuits wherein each output circuit has different data signal coupled to it input. The single delay of AAPA is not explicitly described in detail.

Ashuri, teaches a single output circuit having its own respective adjustable delay (delay shifter 310) providing a respective delayed first clock signal (from external clock 321) to an output circuit (flip-flop 350), wherein each adjustable delay circuit contains a programming circuit (fuses 520 and capacitors 530) for programming a respective delay to be applied to the respective clock signal, and wherein each programming circuit contains at least one fuse element (fuse elements 520) for programming [figures 3 and 5 and corresponding text]. In summary, Ashuri teaches an apparatus having a particular data signal for an output circuit that also has an associated adjustable delay. The invention of Ashuri ensures that a clock signal is delayed by an appropriate amount relative to a delay with associated data signal. Ashuri further implicitly teaches that anti-fuses would be applicable to his invention because in using fuses one of ordinary skill would have readily recognized that anti-fuses would be just as effective in selecting the delay amount either in combination with fuses or in substitution of fuses. Therefore, using fuses and/or anti-fuses does not depart from the scope of Ashuri's invention.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify AAPA by removing the single delay of AAPA and placing a delay as taught by Ashuri

for each output circuit into the respective clock line because both AAPA and Ashuri are directed toward placing data into a clock signal. This modification results in the applicants claimed invention. That is, each output circuit has it own associated adjustable delay circuit. In making the modification the delay for each clock would be equal to a corresponding delay of the data signal. Therefore, in making the modification using the teachings of Ashuri into AAPA would suggest to one of ordinary skill that the each of said respective data signals would be output by said plurality of output circuits at substantially the same time. An artisan would have made the modification because Ashuri teaches that in his invention that a clock signal will (and should) be delayed by an appropriate amount for each data signal. Ashuri further teaches that the adjustable delay for the clock is desirable because it allows the data signal to be sampled at an appropriate time and that the delay is adjustable to accommodate different amounts of propagation delay for a particular data signal [col. 1 lines 21-60].

15. As to claims 42-47 and 49-51, they are rejected on the same basis as set forth hereinabove.

16. As to claim 52, AAPA together with Ashuri taught the data output apparatus according to claim 1 as described above. Ashuri further teaches wherein each of said delay circuits comprises:

a. an input for receiving said first clock signal (input to delay shifter.) [figure 3];

b. a plurality of delay elements (capacitance 530), each of said delay elements providing a respective delay to a signal applied thereto [figure 5 and col. 3 lines 44 et seq.];

c. a switch circuit (fuses and circuitry, which is not shown, for programming the delay) for configuring said delay elements to provide a selected delay to the delayed first clock signal [figure 5 and col. 3 lines 44 et seq.].

In summary, Ashuri further taught an input for receiving a clock and the delay elements provide a respective a selected delay for each circuit.

AAPA together with Ashuri do not expressly disclose that each of the delay elements provide different respective delay. Ashuri does not detail the value of the delay elements within each delay circuit. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of AAPA and Ashuri to use delay circuits with delay elements such as those taught by Ashuri wherein each of the delay elements has a different respective delay. The teaching of Ashuri would suggest to one of ordinary skill in the art that delay values in the delay circuit may be of differing values. One of ordinary skill would want to use differing delay values to apply both coarse (large) and fine (small) delays. Doing so would allow a wide range of delays to be used with desirable accuracy.

Response to Arguments

17. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

18. Applicant's arguments filed 9 September 2004 have been fully considered but they are not persuasive.

19. Applicants argue in substance that Ashuri does "not teach or suggest a plurality of delay circuits wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to a first clock signal such that a plurality if [sp] data signals are output by a respective plurality of output circuits at substantially the same time".

The examiner agrees that Ashuri does not teach or suggest a plurality of delay circuits. That is why reference to AAPA is relied upon to teach this feature.

Ashuri teaches that each output circuit should have a respective adjustable delay circuit containing a programming circuit for programming a respective to be applied to a first clock signal. Specifically, Ashuri teaches at col. 3 lines 13-23, that the programmable delay should be added to the clock signal so that the delay corresponds to the data signal.

When modifying AAPA with the teachings of Ashuri, the modification would have a plurality of delay circuits wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to a first clock signal such that a plurality of data signals are output by a respective plurality of output circuits at substantially the same time.

20. Applicants also argue in substance that Ashuri can be considered as disclosing nothing more than what is already disclosed in AAPA. The examiner disagrees.

Ashuri discloses that the programmable delay of the clock is set be appropriate to the delay in the data signal (col. 3 lines 13-23). AAPA cannot teach this because AAPA has only one delay in the clock signal for a plurality of data signals. Thereofore, the delay cannot be appropriate for each data signal. Thus, Ashuri would provide improvement of AAPA by allowing the data signal to be output at substantially the same time.

Conclusion

21. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (571) 272-3677. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James Trujillo
October 28, 2004

REHANA PERVEEN
PRIMARY EXAMINER
11-1-04